13.5 A 65fJ/Conversion-Step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS

Jan Craninckx, Geert Van der Plas

IMEC, Leuven, Belgium

ADCs with 8b to 10b accuracy operating at several 10s of MS/s have for a long time been the territory of pipeline architectures. But in scaled CMOS, these specifications have become well in range of SAR ADCs. Most SAR ADCs use an operating principle similar to the charge redistribution architecture [1]. This requires fast-settling opamps in both the input and the reference voltages, able to settle their output voltage in a very short time while driving large capacitive loads. Also the high-speed clock for the controller that has to run at 10× the sampling speed must be available. Using the typical FOM definition for ADCs,

$$FOM = \frac{P}{2^{ENOB} \cdot F_S}$$

current state-of-the-art FOM is around 0.2pJ [2, 3], and often this does not take into account the reference buffers or clock generation.

A SAR architecture is proposed that uses passive charge sharing (instead of active charge redistribution) to both sample the input signal and to perform the binary-scaled feedback during the successive approximation. The basic architecture depicted in Fig. 13.5.1 works completely in the charge domain. The input is sampled on a capacitor and during the SAR algorithm, charge is added or subtracted until the result converges to zero. Simple passive switches, instead of any active circuits, are used to add/subtract these charges. The only active element is the comparator itself, which is the basic principle that allows achieving the fundamental lowest limit on power consumption.

The operation of the ADC can be explained with the waveforms shown in Fig. 13.5.2. Before the start of conversion, the sampling capacitors C_S are reset to zero. The tracking switch S_T is closed and the sampling switch S_S is open, so the charge on the tracking capacitors C_T follows the differential input signal. The binary-scaled array of unit capacitors C_U is pre-charged to the power supply. The charge on this capacitor array will be used to provide the feedback DAC function in the SAR ADC, and thus functions as the "reference voltage" in a charge-redistribution SAR. Since this pre-charging happens before the actual A-to-D conversion, it does not depend on the input signal and thus no tough constraints are imposed on this "reference".

The conversion process starts with the sampling of the input signal. Therefore, S_T opens to hold the input and when S_S closes, half of the charge on C_T is transferred to C_S in a simple passive charge-sharing action. The transfer time is proportional to the on-resistance of the switch and therefore, is very short. After sampling, S_S opens and S_T closes, so the input signal can be tracked again. The sampling process typically takes < 2ns, so abundant time is available for tracking and no settling problems occur.

To determine the MSB, the comparator is activated and after its decision, a charge equal to half of the input range is added to or subtracted from the sampled charge. Therefore, one of the signals Cp[0] or Cn[0] goes high, the other one stays low. This is again a passive process that does not take any power and yet settles very fast in an advanced technology. The total charge stored now is equal to $C_S \cdot V_{IN}/2 \pm C_{MSB} \cdot V_{DD}$ and is distributed proportionally across the 2 capacitors. The next bits are determined in a similar operation: the comparator determines the sign of the charge for each iteration, and the binary-scaled pre-charged capacitors are connected one by one to make the total charge converge to zero.

The fundamental power limits of the original architecture are removed by doing all the charge-redistribution passively. The input is connected to the tracking capacitor for most of the conversion period, so no fast opamp is needed for input sampling. Secondly, settling problems in the reference voltage are avoided by pre-charging all capacitors to the same voltage before the conversion process, and this is signal independent. This way the only remaining active element in the ADC is the comparator itself and the digital controller. Another advantage is the fully digital implementation that only requires MOS switches and metal-oxide-metal (MOM) capacitors, making it portable to new CMOS technologies.

Two constraints determine the size of the capacitors. For device mismatch, the total size of the capacitor array must be at least 2pF. Much more stringent however, is the size of the unit capacitor, this must be 2^{N-1} times smaller and thus turns out to be only 8fF. As this is not practical, the capacitor array, shown in Fig. 13.5.3, is designed. A unit capacitor of 64fF is used, but for the 3 LSBs, this one is pre-charged to only a fraction of the full supply voltage. Again, passive charge-sharing is used, as shown by the waveforms in Fig. 13.5.3. With 2pC of charge taken from the reference, the value of C_T and C_S must be 10pF each.

The comparator is shown in Fig. 13.5.4. It is based on [4] and includes a programmable capacitor array to calibrate its offset voltage. The comparator does not consume any power when inactive, and thus the power consumption of the ADC scales linearly with the sampling frequency. The output *Valid* indicates when the comparison is done and it is used by the asynchronous SAR controller as a trigger to continue the conversion process by closing one of the sharing switches. Typical comparison time is about 0.3ns.

To avoid the need for a high-speed clock (and its associated power consumption), an asynchronous controller is implemented. On the rising edge of the input clock, a pulse in the tracking/sampling signal is generated as shown in Fig. 13.5.2. The width of this pulse (~2ns) is proportional to the RC time constant of a MOS switch and a MOM capacitor to track the time required for the charge-sharing sampling process over process variations. Then the conversion process starts that repetitively activates the comparator, waits for the *Valid* signal, closes one of the sharing switches, and waits for another delay (~1ns) while the charge-sharing settles. When this has happened 9 times, the output bits are toggled. The sampling capacitors are then reset and the capacitor array is pre-charged, waiting for the next input clock edge. The total conversion time is about 20ns, so the maximum conversion rate of the ADC is 50MS/s.

A die micrograph of the charge-sharing SAR ADC implemented in 90nm 1P9M digital CMOS is shown in Fig. 13.5.7. The total area of the chip is 1.2×1.1mm² and the ADC core is 400×200µm². At 50MS/s, the chip draws 0.7mA from a 1V supply, divided over different blocks as follows: digital 50%, comparator 35%, pre-charging 15%. Measured INL and DNL at 50MS/s are below 0.6LSB, as shown in Fig. 13.5.5. Despite this good linearity, the SNDR for low-frequency input signals is 49dB (ENOB=7.8), because it is limited by underestimated comparator noise. At frequencies above 10MHz, the nonlinearity of the input tracking switch becomes dominant because the low-V_t transistors intended to be used were not processed correctly. This deteriorates the ENOB for a near-Nyquist input at 20MS/s to 7.4, as shown in Fig. 13.5.6. Consuming 290µW, the resulting FOM is 65fJ/conversion-step. As none of the ADC building blocks consumes any static power, the FOM is maintained down to very low conversion rate.

References:

[1] J. McCreary and P. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques - Part I," *IEEE J. Solid-State Circuits*, vol. 10, no. 6, pp. 371-379, Dec., 1975.

[2] N. Verma and A. Chandrakasan, "A 25µW 100kS/s 12b ADC for Wireless Micro-Sensor Applications", *ISSCC Dig. Tech. Papers*, pp. 222-223, Feb., 2006

[3] S. Chen and R. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 574-575, Feb., 2006

[4] G. Van der Plas, S. Decoutere and S. Donnay, "A 0.16pF/conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process", *ISSCC Dig. Tech. Papers*, pp. 566-567, Feb., 2006.

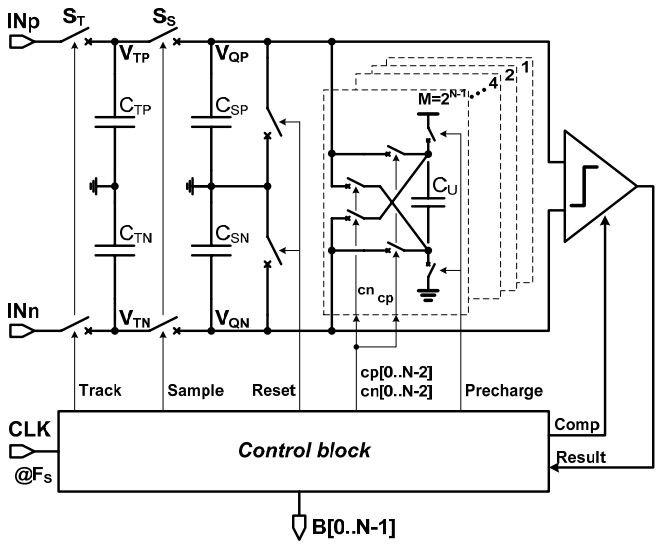

Figure 13.5.1: Basic charge-sharing SAR ADC architecture.

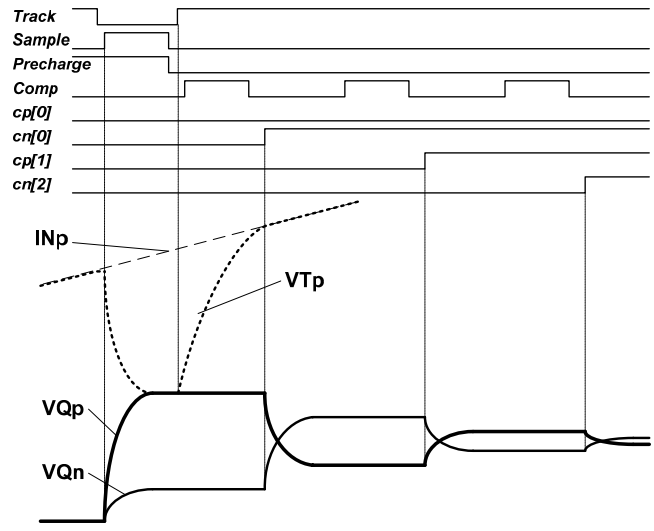

Figure 13.5.2: Charge-sharing SAR ADC waveforms.

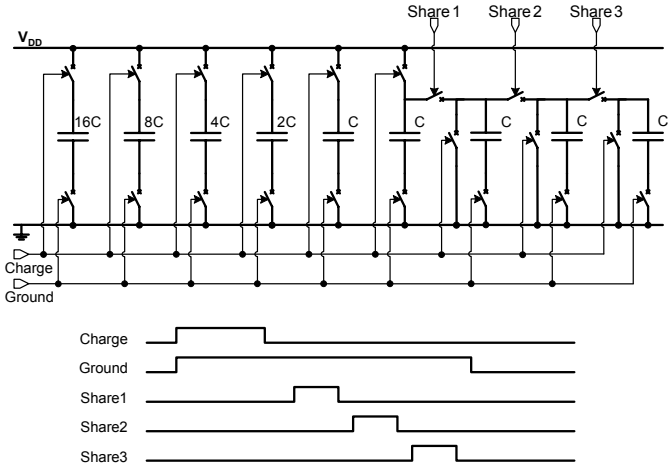

Figure 13.5.3: Modified capacitor array.

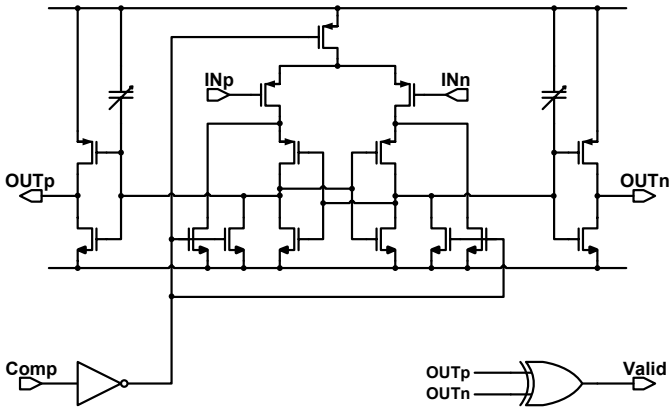

Figure 13.5.4: Comparator circuit schematic.

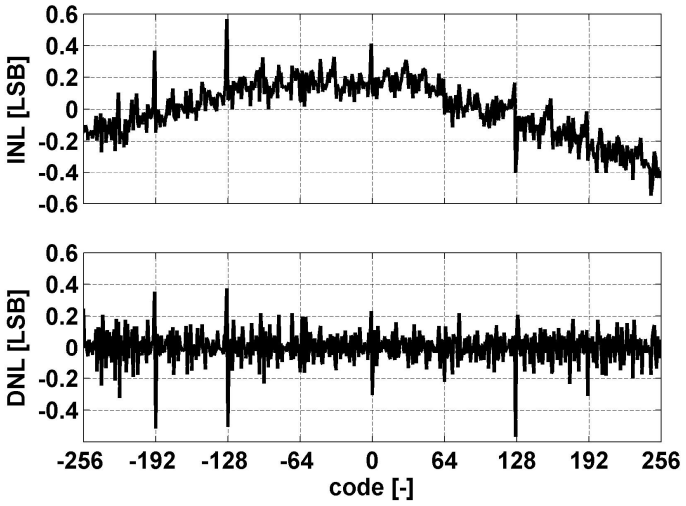

Figure 13.5.5: INL/DNL plot at 50MS/s.

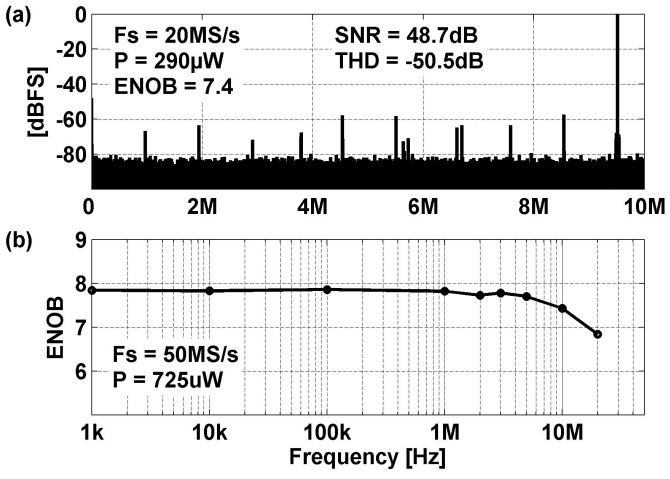

Figure 13.5.6: (a) Near-NyquistFFT at 20MS/s; (b) ENOB vs. input frequency at 50MS/s.

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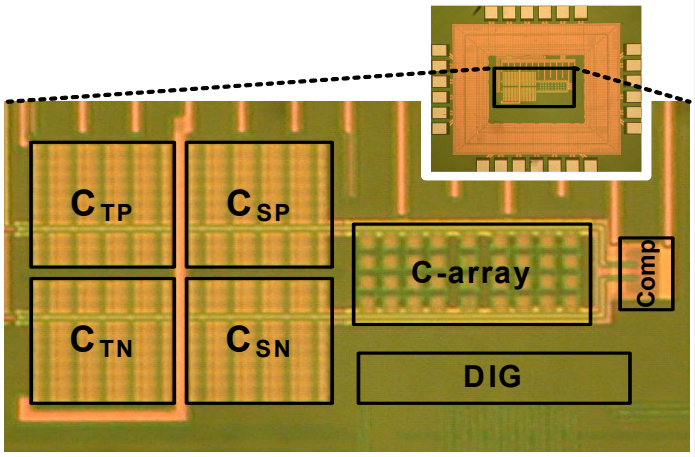

Figure 13.5.7: Die micrograph.

